

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of : Customer Number: 20277
Kazuya YAMAMOTO, et al. : Confirmation Number:
Serial No.: Divisional of Appl. No.
09/902,102 : Group Art Unit:
Filed: January 22, 2004 : Examiner:
For: SEMICONDUCTOR DEVICE WITH BIPOLAR TRANSISTOR DEVICE

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The references were cited by or submitted to the U.S. Patent and Trademark Office in parent application Serial No. 09/902,102, filed July 11, 2001, which is relied upon for an earlier

Serial No.: Divisional of Appl. No.

filings date under 35 USC 120. Thus, copies of these references are not attached. 37 CFR
1.98(d).

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Respectfully submitted,

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)			ATTY. DOCKET NO. 57454-991	SERIAL NO. Divisional of Appl. No. 09/902,102			
			APPLICANT Kazuya YAMAMOTO, et al.				
			FILING DATE January 22, 2004	GROUP			
U.S. PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ₂ (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document			
	US	6,278,328 B1	08/21/2001	Yamamoto			
	US	5,629,648	05/13/1997	Pratt			
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FOREIGN PATENT DOCUMENTS							
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number +-Kind Codes (<i>if known</i>)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
		JP 11-186282	07/09/1999	TOSHIBA CORP.			
		JP 9-181086	07/11/1997	HITACHI LTD., HITACHI MICROCOMPUT SYST. LTD.			
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		GB 965,421 (Counterpart of FR 1,272,819)	07/29/1964	TELEFUNKEN GMBH			
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
		YAMAMOTO et al. "A 3.2-V Operation Single-Chip Dual-Band AlGaAs/GaAs HBT MMIC Power Amplifier With Active Feedback Circuit Technique", IEEE JOURNAL OF SOLID STATE CIRCUITS, Vol. 35, No. 8, August 2000, pp. 1109-1120.					
		VON GEORG ORTLER, "Parallel Connected Transistors in the Inverse Mode", FREQUENZ., Vol. 35, No. 8 (August 1981) pages 215-219.					
EXAMINER				DATE CONSIDERED			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.